Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1 and 18 have been amended. No claims have been cancelled. Therefore, claims 1-26 are presented for examination.

Claims 1-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Venkitakrishnan et al. (U.S. Patent No 2003/0023794). Applicants submit that the present claims are patentable over Venkitakrishnan.

Venkitakrishnan discloses a CMP system. The CMP system includes processor units coupled to a system bus. Each of processors has its own clock, cache and program counter. An external interface unit, an embedded RAM unit, and an arbiter unit are also coupled to bus. All of the above components are fabricated into a single integrated circuit die. See Venkitakrishnan at [0023] – [0024]. Venkitakrishnan also discloses a Copy Forward (CF) message which involves cache to cache transfers ([0091]).

Claim 1 of the present application recites control logic coupled to first and second dedicated caches to receive first data from the first dedicated cache and to transfer the first data to the second dedicated cache entirely within the integrated circuit. Applicants submit that nowhere in Venkitakrishnan is there disclosed control logic that receives data from a first cache and transfers the data to a second cache. Therefore, claim 1 is patentable over Venkitakrishnan.

Claims 2-11 depend from claim 1 and include additional features. Thus, claims 2-11 are also patentable over Venkitakrishnan.

Claim 12 recites a process of transferring first data from a first dedicated cache of a chip multi-processor to control logic in the chip multi-processor, entirely within the chip

multi-processor; and subsequently transferring the first data from the control logic to a second dedicated cache of the chip multi-processor, entirely within the chip multi-processor. Thus, for the reasons described above with respect to claim 1, claim 12 is also patentable over Venkitakrishnan. Since claims 13-17 depend from claim 12 and include additional features, claims 13-17 are also patentable over Venkitakrishnan.

Claim 18 recites control logic coupled to first and second dedicated caches to receive first data from the first dedicated cache and to transfer the first data to the second dedicated cache entirely within the integrated circuit. Accordingly, for the reasons described above with respect to claim 1, claim 18 is also patentable over Venkitakrishnan. Because claims 19-22 depend from claim 18 and include additional features, claims 19-22 are also patentable over Venkitakrishnan.

Claim 23 recites transferring first data from a first dedicated cache of a chip multi-processor to control logic in the chip multi-processor, entirely within the chip multi-processor; and subsequently transferring the first data from the control logic to a second dedicated cache of the chip multi-processor, entirely within the chip multi-processor. Therefore, for the reasons described above with respect to claim 1, claim 23 is also patentable over Venkitakrishnan.

Since claims 24-26 depend from claim 23 and include additional features, claims 24-26 are also patentable over Venkitakrishnan.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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